CLAIMS

We claim:

1. A computer system comprising:

a system controller including a central processing unit and a memory bus controller and configured to operate in a first interface mode;

a system memory connected with the system controller through the system bus;

a NAND flash memory configured to store a system driving code, an operating system program, and user data for the computer system; and

an interface unit configured to communicate with the system controller through the system bus in the first interface mode and configured to communicate with the NAND flash memory in a second interface mode, the interface unit being synchronized with a clock signal generated in response to predetermined command information.

2. The computer system of claim 1, wherein the interface unit comprises:

a host interface unit configured to communicate with the system controller through the system bus in the first interface mode;

a register unit configured to store configuration information about the computer system, the NAND flash memory, and the command information;

a buffer unit for configured to store data of the NAND flash memory;

an oscillator configured to generate the clock signal in response to the command information;

a state machine synchronized with the clock signal and configured to control an inner operation of the interface unit in response to the command information; and

a NAND flash interface unit synchronized with the clock signal and configured to communicate with the NAND flash memory via the state machine in the second interface mode.

3. The computer system of claim 2, wherein the interface unit further comprises a power-up detector configured to apply a power sensing signal to the state machine when power is applied.

4. The computer system of claim 3, wherein the interface unit further comprises an error correcting circuit synchronized with the clock signal and configured to perform an error test and correction on the data of the NAND flash memory.

5. The computer system of claim 4, wherein the state machine comprises:

a first block configured to control operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block configured to control an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block configured to control an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block configured to control an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and configured to control an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

6. The computer system of claim 5, wherein the state machine further comprises:

a fifth block configured to control an operation to erase the data stored in the NAND flash memory; and

a sixth block configured to apply a reset command to the NAND flash memory and to a plurality of registers within the interface unit.

7. The computer system of claim 1, wherein the interface unit comprises:

a first interface unit configured to communicate with the system controller through the system bus in the first interface mode;

a second interface unit synchronized with the clock signal and configured to communicate with the NAND flash memory in the second interface mode;

a storage unit configured to store information and data exchanged between the first and second interface units; and

a control unit synchronized with the clock signal and configured to control a transmission of the information and data between the first and second interface units.

8. The computer system of claim 7, wherein the storage unit comprises:

a register unit configured to store configuration information about the computer system, the NAND flash memory, and the command information about the NAND flash memory; and

a buffer unit configured to store data of the NAND flash memory.

9. The computer system of claim 7, wherein the interface unit further comprises a power-up detector configured to apply a power sensing signal to the state machine when power is applied.

10. The computer system of claim 9, wherein the interface unit further comprises an error correcting circuit synchronized with the clock signal and configured to perform an error test and correction on the data of the NAND flash memory.

11. The computer system of claim 7, wherein the control unit comprises:

a first block configured to control operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block configured to control an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block configured to control an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block configured to control an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and configured to control an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

12. The computer system of claim 11, wherein the control unit further comprises:

a fifth block configured to control an operation to erase the data stored in the NAND flash memory; and

a sixth block configured to apply a reset command to the NAND flash memory and to a plurality of registers within the interface unit.

13. A booting method for a computer system with a NAND flash memory comprising:

copying a system bootstrap code to a buffer from the NAND flash memory in response to a power applying detecting state;

initializing the computer system according to the system bootstrap code stored in the buffer;

copying an operating system code to a programmable memory from the NAND flash memory; and

executing the operating system code.

14. A method for reading out data from a NAND flash memory in a computer system having a system controller and a buffer, the method comprising:

setting commands, addresses, and pages to be read out from the NAND flash memory;

copying data of a first page from the NAND flash memory to the buffer; and

copying data of a second page from the NAND flash memory to the buffer while transmitting the first page data from the buffer to the system controller.

15. The method of claim 14, further comprising:

copying data of a N^{th} page to the buffer from the NAND flash memory while transmitting data of a $(N-1)^{th}$ page until the copying of all the pages is completed.

16. The method of claim 14, wherein the data of the pages is transmitted successively.

17. A method for programming data from a NAND flash memory in a computer system with a system controller and a buffer, the method comprising:

setting commands, addresses, and pages to be programmed to the NAND flash memory;

successively loading data necessary for the pages to be programmed from the system controller to the buffer; and

sequentially programming the pages by using the data loaded to the buffer.

18. The method of claim 17, wherein sequentially programming the pages comprises:

programming data from one page while the data for another page is being successively loaded to the buffer.